

CLAIMS

What we claim is:

- 1 1. A method comprising:
 - 2 determining at least one characteristic of a first input/output (I/O) device that is
 - 3 coupled to a memory device interface, the memory device interface being
 - 4 configured to enable data transfers between the I/O device and a memory
 - 5 device; and
 - 6 buffering data corresponding to the first I/O device in a first portion of a buffer of the
 - 7 memory device interface, a size of the first portion being responsive to the at
 - 8 least one characteristic of the first I/O device.
 - 1 2. The method of claim 1, further comprising:
 - 2 determining at least one characteristic of a second I/O device that is coupled to the
 - 3 memory device interface; and
 - 4 buffering data corresponding to the second I/O device in a second portion of the
 - 5 buffer, a size of the second portion being responsive to the at least one
 - 6 characteristic of the second I/O device.
 - 1 3. The method of claim 2, further comprising:
 - 2 receiving data from the first I/O device via a first data transfer link; and
 - 3 receiving data from the second I/O device via a second data transfer link.
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- 1 4. The method of claim 2, further comprising:
 - 2 receiving a first data unit from the first I/O device;
 - 3 buffering the first data unit in the first portion of the buffer; and
 - 4 transferring the first data unit to the memory device;
 - 5 receiving a second data unit from the second I/O device;
 - 6 buffering the second data unit in the second portion of the buffer; and
 - 7 transferring the second data unit to the memory device.

1 5. The method of claim 1, wherein the at least one characteristic comprises at least one of:
2 a rate at which the I/O device is able to read data from the memory device;
3 a rate at which the I/O device is able to write data to the memory device;
4 a bandwidth of a link coupled between the I/O device and the memory device
5 interface;
6 a size of a data unit that the I/O device reads from the memory device per read
7 request;
8 a size of a data unit that the I/O device writes to the memory device per write request;
9 a tolerance that the I/O device has for a delay by the memory device interface in
10 fulfilling a write request; or
11 a tolerance that the I/O device has for a delay by the memory device interface in
12 fulfilling a read request.

1 6. A method for allocating buffer capacity in a memory device interface that is configured to
2 transfer data between an input/output (I/O) device and a memory device, the method
3 comprising:
4 buffering data received via a first data transfer link in a first portion of a buffer of the
5 memory device interface;
6 buffering data received via a second data transfer link in a second portion of the
7 buffer, a buffering capacity of the first portion being different than a buffering
8 capacity of the second portion.

1 7. The method of claim 6, wherein the buffering capacity of the first portion is responsive to
2 at least one characteristic of a first I/O device that provides data to the memory device
3 interface via the first data transfer link, and the buffering capacity of the second portion is
4 responsive to at least one characteristic of a second I/O device that provides data to the
5 memory device interface via the second data transfer link.

1 8. The method of claim 7, further comprising:
2 receiving a first data unit from the first I/O device via the first data transfer link;

3 buffering the first data unit in the first portion of the buffer;
4 transferring the first data unit to the memory device;
5 receiving a second data unit from the second I/O device via the second data transfer
6 link;
7 buffering the second data unit in the second portion of the buffer; and
8 transferring the second data unit to the memory device.

1 9. The method of claim 7, further comprising:

2 receiving a first data unit from the memory device;
3 buffering the first data unit in the first portion of the buffer;
4 transferring the first data unit to the first I/O device;
5 receiving a second data unit from the memory device;
6 buffering the second data unit in the second portion of the buffer; and
7 transferring the second data unit to the second I/O device.

1 10. A memory device interface that is configured to enable data transfers between an
2 input/output (I/O) device, the memory device interface comprising:

3 a buffer;
4 a first plurality of registers that are configured to enable the memory device interface
5 to buffer in a first portion of the buffer data corresponding to a first I/O
6 device; and
7 a second plurality of registers that are configured to enable the memory device

8 interface to buffer in a second portion of the buffer data corresponding to a
9 second I/O device, a size of the first portion of the buffer being different than
10 a size of the second portion of the buffer.

1 11. The memory device interface of claim 10, wherein the buffer comprises random access
2 memory (RAM).

- 1 12. The memory device interface of claim 10, wherein the first plurality of registers
2 comprises:
3 a first buffer allocation counter that specifies a buffer allocation value that is
4 configured to enable data received from the first I/O device to be buffered in
5 the first portion of the buffer; and
6 a second buffer allocation counter that specifies a buffer allocation value that is
7 configured to enable data received from the second I/O device to be buffered
8 in the second portion of the buffer.
- 1 13. The memory device interface of claim 12, wherein the value of the first buffer allocation
2 counter is decremented responsive to a buffer allocation value being sent to the first I/O
3 device.
- 1 14. The memory device interface of claim 13, wherein the value of the first buffer allocation
2 counter is incremented responsive to data being read from the first portion of the buffer.
- 1 15. A memory device interface comprising:
2 a buffer;
3 a first plurality of registers that are configured to enable the memory device interface
4 to buffer in a first portion of the buffer data received via a first data transfer
5 link; and
6 a second plurality of registers that are configured to enable the memory device
7 interface to buffer in a second portion of the buffer data received via a second
8 data transfer link, a size of the first portion of the buffer being different than a
9 size of the second portion of the buffer.
- 1 16. The memory device interface of claim 15, wherein the buffer comprises random access
2 memory (RAM).

1 17. The memory device interface of claim 15, wherein the first data transfer link is coupled
2 to a first input/output (I/O) device, and the second data transfer link is coupled to a second
3 I/O device.

1 18. The memory device interface of claim 15, wherein the first plurality of registers
2 comprises:
3 a first buffer allocation counter that is configured to enable data received via the first
4 data transfer link to be buffered in the first portion of the buffer; and
5 a second buffer allocation counter that is configured to enable data received via the
6 second data transfer link to be buffered in the second portion of the buffer.

1 19. A system comprising:
2 means for determining at least one characteristic of a first input/output (I/O) device
3 that is coupled to a memory device interface, the memory device interface
4 being configured to enable data transfers between the I/O device and a
5 memory device; and
6 means for buffering data corresponding to the first I/O device in a first portion of a
7 buffer of the memory device interface, a size of the first portion being
8 responsive to the at least one characteristic of the first I/O device.

1 20. The system of claim 19, further comprising:
2 means for determining at least one characteristic of a second I/O device that is
3 coupled to the memory device interface; and
4 means for buffering data corresponding to the second I/O device in a second portion
5 of the buffer, a size of the second portion being responsive to the at least one
6 characteristic of the second I/O device.